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NHi-15530 ISA MIL-STD-1553 IDEA MKIII TESTER CARD



FEATURES

- Simulates Bus Controller, 31 independent Remote Terminals and Monitor
- BC supports up to 250 independent messages
- Messages are organized in a frame with up to 1000 entries
- Message timing is accurate to within 4 microseconds
- The BC and RTs share 250 data tables
- Error injection includes all types required for SAE RT validation
- 1553 dual transceiver has programmable amplitude and rise time
- Software supports up to 8 cards in the same PC
- Extensive run-time-library and user friendly menus for Windows NT/2000/XP

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NHi-15530 ISA MIL-STD-1553 IDEA MKIII Tester Card

Functional Description

The NHi-15530 MKIII is an ISA bus compatible card, which functions as a tester/simulator for MIL-STD-1553 systems. The card concurrently emulates a Bus Controller, up to 31 independent Remote Terminals and a Bus Monitor.

The Bus Controller supports up to 250 independent messages and data tables. The messages are organized in a frame which holds up to 1000 entries; both major and minor frame periodicities are supported and timing is accurate to within 4 microseconds.

The Remote Terminals support up to 250 data tables which are accessed as a function of the command's terminal address, T/R bit and subaddress. Each of the 31 Remote Terminals has its own unique status which is dynamically updated as required by MIL-STD-1553. Protocol options such as broadcast, legality detection and dynamic bus control are supported. In addition, each Remote Terminal has its own error injection definition and can be used to thoroughly test external Bus Controllers.

The intelligent Bus Monitor is triggered by error type, command type, bits set in status words or an external TTL input. Messages are selected according to the command fields: terminal address, T/R bit and subaddress as well as the bus ID. The Monitor detects and reports all errors defined by MIL-STD-1553B and supports sustained real-time storage to disk of messages from a fully loaded bus.

The card has outstanding error injection capability and provides all the errors defined by the SAE Validation Test Plan for Remote Terminals. These capabilities include: encoding errors such as sync/parity/half-bit inversion, length errors (words per message and bits per word), gap errors, zero-crossing errors, and response errors. A unique feature of the card is the ability to inject glitches to simulate the most common source of errors encountered during a noise test. The card's proprietary dual redundant transmitter has programmable rise times ranging from less than 100 nanoseconds to more than 250 nanoseconds and the amplitude can be varied from 0 to over 28 $\rm V_{pp}$ across 75 ohms.

The board contains eight 8K x 16 pages of shared memory which can be mapped to any 32 KB block from 640K to 16M in the ISA bus address space. The offset in the host address space and the interrupt request line are programmed by writing to I/O registers, thus eliminating the need for switches.

User-friendly menus for interactive operation as well as an extensive run-time library (RTL) for customer developed applications are supplied with the card. These packages run under DOS and Windows 3.X/95/NT. The RTL contains over 100 functions written in Microsoft C/C++ and complies with VISA software conventions to facilitate platform portability. The library compatible with Visual Basic 4 and LabWindows 4.0 as well as the Venturcom RTX real-time extension for NT. Support is provided for double-buffered data tables and message frames, queued interrupts, block data transfers via 1553, and over 30 special routines executed by the board's BC/RT during intermessage gaps. Data structures can be created, tested and saved using the menu software and then imported by the library. The run-time library is therefore an ideal tool for highly efficient sophisticated real-time applications.

Two very useful software packages are included without additional cost. The first program is a powerful Parameter Monitor for real-time or off-line analysis and display of data in graphical form. The second program is a Communication Reconstructor which facilitates system integration by replaying previously monitored messages with the original contents and timing.

Software packages for executing the complete Validation and Production Test Plans defined by the SAE are available as options. The programs are exceptionally efficient; a complete Production protocol test executes in less than 20 seconds and the Validation protocol test executes in less than 1 hour.



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SPECIFICATIONS

Bus Controller

Number of Messages	up to 250
Message Timing	determined by a 32 bit timer with 2 microsecond resolution, major/minor frame periodicity supported, asynchronous insertion of messages supported
Message Frame Size	up to 1000 entries
Data Tables	up to 250 tables shared with emulated Remote Terminals
Input Trigger	wait until next message when TTL input is low
Output Trigger	active high TTL pulse after start of major frame

Remote Terminals

Number of Remote Terminals	up to 31
Data Tables	up to 250 tables shared with Bus Controller
Status Words	individual status words for each Remote Terminal,
	dynamic update of message error and broadcast bits
Protocol Options	legality detection, broadcast and dynamic bus control as per
·	1553

Bus Monitor

Storage Triggering	immediate or
	specified commands/bits set in status/error type
Message Selection	any subset of commands based on terminal address, T/R bit
	and subaddress
Time Tag	32 bits with 2 microsecond resolution
Input Trigger	initiate message storage when TTL input is high
Output Triggers	active high TTL output after detection of storage trigger,
	active high TTL output after detection of invalid message
Real Time Display	matrix of 8 counters per terminal address displaying
	message exceptions and total message count
Error Detection/Reporting	invalid command/data/status, late/early response, wrong
	terminal address, gap/missing word, inverse sync, flagged
	status bit

Error Injection

Error injection	
Inverse Errors	signal inversion starting on any 50 nanosecond boundary for up to 3 microseconds (used to inject inverted sync, inverted parity and inverted half-bits)
Glitch Errors	same timing as Inverse Errors
Gap Errors	1, 2 or 3 microseconds between neighboring words
Zero-crossing Errors	-250 to +250 nanoseconds with better than 1 nanosecond resolution (available with Validation Test software)
Message Length Errors	1 to N words (N=nominal number of words)
Word Length Errors	± 3 , ± 2 , or ± 1 , bits in any word
Response Errors	no response, late response of 12 to 30 microseconds in 1 microsecond steps, response on alternate bus, response with wrong terminal address

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Miscellaneous

Transmit Amplitude	0 to 28 V _{pp} (min) in 256 steps
Transmit Rise/Fall Time	<100, 140-180, 180-220, or >250 nanoseconds
Response Timeout	14, 16, 18 or 20 microseconds

Connectors

Triax x 2	transformer coupled stubs for A and B buses, Trompeter BJ77 (or equivalent)
25 pin D-type	Bus Controller: 4 inputs and 4 outputs, TTL compatible,
	Bus Monitor: 4 inputs and 4 outputs, TTL compatible,
	direct coupled stubs for A and B buses

Host Interface Requirements

Bus	16 bit ISA (IBM/PC compatible)
Memory	any 32 KB block above 640 K (selected by I/O)
Interrupt	IRQ 5, 10, 11 or 12 (selected by I/O)
I/O	any 4 byte block (selected by DIP switch)

Power Requirements

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5 volts	1.7 A (max)
12 volts	15 mA @ 0% transmit duty cycle
	400 mA (max), @ 100% transmit duty cycle, 28 V _{pp} output
-12 volts	55 mA (max)

Environmental Conditions

Operating Temperature Range	0 to 50° C
Storage Temperature Range	-20 to 70° C
Humidity	0 to 30 % non-condensing
Size	Half- length IBM/PC AT compatible (122.2 mm x 171.5 mm)







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