Data Device Corporation

Multi-Terminal CCPMC Card

NHi-15505
Instructions

Version 1.0
May 2004

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1.0 Package Contents

One CCPMC card
Instructions
Software Disks: WindowsNT/XP/98/2000 Flight Deck Software
RunTime Library
NHi-156XXMan.pdf

Flight Deck is menu driven GUI software For a PC which controls the CCPMC card and all the functions of the multi-protocol terminals on the card.

Optional PMC to PCI adapter card is required when Flight Deck is used in a PC.
They are available through Companies such as:

Catalyst Enterprises Inc 408-365-3848
Dynamic Engineering 831-336-8891

NHi-156XXMan.pdf is the manual for the NHi-15650ET terminals which are used on the card.

1.1 CCPMC FEATURES

- Mil-Std-1553 and Multi-protocol PCI Interface Card
- Up to four Independent Multi-protocol BC/RT/MT/MT-RT on the card
- Conduction Cooled
- 33/66 MHz operation
- Military temperature range
- Independent BC triggers
- External time tag

1.2 GENERAL TERMINAL FEATURES

- Multi-Protocol Interface
- Operates from 20 Mhz clock.
- Appears to host as a Dual Port Double Buffered 64K x 16 SRAM
- Footprint less than 1 square inch
- Ensures integrity of all shared data and control structures
- Built- in interrupt controller
- Internal FIFO is configurable to retain header information for queuing up to 6 pending interrupt requests plus an overflow interrupt, or as a 7 interrupt revolving FIFO
- 32 bit RTC (Real- Time- Clock) for time taging with 1, 2, 4, 8,1 6, 32 and 64 uS selectable tick rate, for data and event time tagging.
- Selectable 768/ 672 us Failsafe Timer with complete Testability.
- Double buffering of messages and data tables.
- Low power CMOS technology

1.2.1 BUS CONTROLLER FEATURES

- Implements all Message Formats and Error Checking
- Major and minor frame message structure.
- Simple setup and operation. Multiple minor frames, message tables and data tables. Only one Major Frame Pointer Register is required to control unlimited number of messages
- BC initialized by writing to three Configuration Registers and the Interrupt Mask Register
- Executes lists of messages via Minor Frame Pointers
- Configurable Global Retry and Message Specific Local Retry
- Programmable retries per message:
  - None
  - Retry Current Bus
  - Retry Alternate Bus
  - Retry Alternate Bus then Current Bus.
- Programmable response timeout of 14, 18, 26, or 42 microseconds.
- Programmable Intermessage Gap Time up to 4 mS with 2uS resolution.
- Programmable Synchronous Message Time up to 4mS with 2uS resolution.
- Extended Gap Time and Synchronous Message Time using NO- OP Feature.
- Programmable Minor Frame Gap with 64 us resolution.
- Programmable Interrupts for:
  - End of Message
  - End of Frame
  - Response Time Out, Message
  - Error
  - Message Retry
  - RT Status Bit Set
  - FIFO Overflow.
- Host controlled commands:
  - Start BC
  - Continuous Mode
  - Stop at End of Message
  - Stop at End of Frame
  - Abort,
  - GOTO Alternate Frame.
- Dynamic Message Bus Switch Upon Successful Retry.
- Synchronous or Asynchronous Messages.
- Synchronous or Asynchronous Minor Frames.
- Up to 63 autonomous data tables per message.

1.2.2 REMOTE TERMINAL FEATURES

- Up to 63 autonomous data tables per message.
- Multiple and individual message logs provide expedited message analysis.
- Asynchronous Message Handling.
- Dynamic Bus Control Acceptance
- Message Illegality is internally programmable.
- Employs data tables with individual tag words which indicate data validity, data latency, table status and broadcast
- Optionally sets the subsystem flag bit whenever stale data is transmitted or received data is overwritten.
- Issues interrupts on any subset of T/ R bit, subaddresses, mode commands, broadcast messages and errors.
- Optionally resets the real- time clock in response to a "Synchronize" mode command.
- Optionally updates the lower 16 bits of the real- time clock in response to a "Synchronize With Data" command.
- Internally loops- back messages under host control for test purposes.
- Employs a decoder algorithm which ensures high noise immunity and a low error rate.
- Software RT Address Lockout.
- MDC3818 Status Response, Error Handling, Status Bit Definition, Mode Code Operation.
- Separate Broadcast Tables and Interrupts.

1.2.3 BUS MONITOR FEATURES

- Simple setup and operation
- Preset multiple data blocks.
- Only one MT Data Start Address Register is required to control unlimited number of message blocks. The data block sizes and locations are totally programmable.
- MT initialized by writing to three MT Configuration Registers and the MT Interrupt Mask Register.
- Error detection and reporting
- All encoding, timing and protocol errors defined by the Protocols are detected.

- Programmable Monitor Modes:
  - Word Monitor, transfers all data with/ without ID and Time Tag words.
  - Message Monitor, transfers all Command and Status words with/ without ID and Time Tag，while data words are transferred directly to conserve memory space.
- Concurrent Bus Monitor and Remote Terminal operation.
- Selective Message Monitor, based on RT Address.
- Programmable Interrupt for End of Block.

1.3 Description

The NHi-15505 is a CCPMC card which contains up to four completely independent 1553 terminals. The terminal is an NHi-15650ET multi-protocol MCM . which can operate as an RT, BC, MT or MT-RT.

All modes of operation access data tables via pointers residing in RAM which facilitates multiple buffering. This allows buffers to change without moving data and promotes efficient use of RAM space. The data tables have programmable sizes and locations.

The invisibility of memory when the card is not present prevents inadvertent access during power-on-self test of the PC or by any other process.

2.0 PC INSTALLATION

The card has been thoroughly tested and inspected before shipment. After removing the card from the packing container, please retain the container as it may be used to store the card when not installed in the computer. The packing container may be utilized in the event that the card has to be returned due to failure or damage.

2.1 System Requirements

PC with PCI Bus
Windows2000/XP/98/NT
Hard disk
Color Monitor

Follow these precautions before installing the card inside your PC. Remove power to the PC before opening the top cover. Install the zero ohm resistors if required for your application as detailed in this manual and then plug the card into an available slot on the motherboard. :

Follow the driver installation instructions in the TXT file associated with each operating system driver.

REMOVE POWER TO THE PC WHEN REMOVING OR INSERTING THE CARD INTO THE PC.

2.2 Hardwired RT Address

The Terminal can be given a unique Remote Terminal(RT) hardwire address via the Pn4 connector.

2.3 PN4 CONNECTOR

The following table lists the PN4 connector functions.

Pin	Function	Pin	Function
1	RT2_ADRP	2	RT1_ADRP
3	GND	4	RT1_ADR4
5	RT3_ADR4	6	RT1_ADR3
7	RT3_ADR3	8	RT3_ADRP
9	RT3_ADR2	10	BCUTRG_L3
11	RT3_ADR1	12	SSF_TF_L3
13	RT3_ADR0	14	RT1_ADR2
15	GND	16	BUSA2_L
17	BCUTRG_L2	18	BUSA2_H
19	GND	20	
21	RT2_ADR4	22	BUSB2_L
23	GND	24	BUSB2_H
25	GND	26	GND
27	BUSB3_H	28	BUSA3_L
29	RT4_ADRP	30	BUSA3_H
31	GND	32	BUSB3_L
33	GND	34	GND
35	RT4_ADR4	36	BUSB1_L
37	GND	38	BUSB1_H
39	RT2_ADR0	40	GND
41	RT4_ADR2	42	RT4_ADR1
43	RT2_ADR1	44	RT1_ADR1
45	RT4_ADR0	46	RT4_ADR3
47	RT2_ADR2	48	RT1_ADR0
49	GND	50	BUSA1_L
51	RT2_ADR3	52	BUSA1_H
53	SSF_TF_L1	54	SSF_TF_L2
55	GND	56	BCUTRG_L1
57	GND	58	BCUTRG_L4
59	X_TMTG_H	60	SSF_TF_L4
61	BUSB4_L	62	BUSA4_L
63	BUSB4_H	64	BUSA4_H

2.4 ZERO OHM RESISTORS

The Zero Ohm Resistors Must Be Installed to connect the respective signals to the Pn4 Connector.

FUNCTION	DESIGNATION	BOARD LOCATION
BCUTGR_L1:	R12	TOP
BCUTGR_L2:	R22	TOP
BCUTGR_L3:	R32	BOTTOM
BCUTGR_L4:	R42	BOTTOM
SSF_TF_L1:	R13	BOTTOM
SSF_TF_L2:	R23	BOTTOM
SSF_TF_L3:	R33	BOTTOM
SSF_TF_L4:	R43	BOTTOM
X. TMTG_H	R9	BOTTOM

3.0 ADDRESS MAP

The following memory map information is required by a user when custom software is being developed for the NHi CCPMC card.. The NHi Flight Deck Windows software handles all memory allocation and accesses.

3.1.0 PCI CONFIGURATION SPACE

ADDRESS(hex)	DATA(hex)	REGISTER
00000000	1758	Vendor Id
00000002	5625	Device Id
00000004	0002	Command
00000006	0400	Status
00000008	00	Revision Id
000000009	00	Program Id
0000000A	80	Sub Class
0000000B	07	Base Class
0000000C	00	Cache Line Size
0000000D	00	Latency Timer
0000000E	00	Header Type
00000010	FFC00000	Base Address
00000014	000000000	Base Address
00000018	00000000	Base Address
0000001C	00000000	Base Address
00000020	00000000	Base Address
00000024	00000000	Base Address
00000028	00000000	Card Bus CIS Pointer
0000002C	1758	Subsystem Vendor Id
0000002E	5625	Subsystem Id
00000030	00000000	Expansion Rom
00000034	0000	Capabilities Pointer
0000036	0000	Reserved
00000038	00000000	Reserved
000003C	00	Interrupt Line
0000003D	01	Interrupt Pin
000003E	00	Min_Gnt
000003F	00	Max_Lat

3.1.1 PCI BASE ADDRESS

Base address register 0x10 is used to store the PCI memory base address. If 0xFFFFFFFF Is written to this base address register, 0xFFC00000 will be read back. This reserves 4 Mb of PCI memory space for the terminal.

The PCI controller will assign a base address to the card. This base address will be in the range 0x00400000 to 0xFFC00000.

3.1.2 PCI ADDRESSING

Each of the four terminals on the card is identified by a terminal Ident which is added to the PCI base address. There is also an Ident to a Card Register which contains information about each of the four terminals on the card. The hexidecimal Ident for each entity is:

ENTITYl	IDENT
Terminal 1	0
Card Register	0XC0000
Terminal 2	0X100000
Terminal 3	0X200000
Terminal 4	0x300000

3.1.3 CARD REGISTER

31	30	29	28	27	26	25	24
DTACK4	DTACK3	DTACK2	DTACK1	0	0	0	0

23	22	21	20	19	18	17	16
0	0	0	0	TER4	TER3	TER2	TER1

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
0	0	0	0	IRQ4	IRQ3	IRQ2	IRQ1

IRQ1: **Bits0**

1 = Interrupt request from terminal 1

IRQ2: **Bits1**

1 = Interrupt request from terminal 2

IRQ3: **Bits2**

1 = Interrupt request from terminal 3

IRQ4: **Bits3**

1 = Interrupt request from terminal 4

RESERVED **Bits4-15**

TER1 **Bits16**

1 = Terminal 1 NOT installed

0 = Terminal 1 installed

TER2 **Bits17**

1 = Terminal 2 NOT installed

0 = Terminal 2 installed

TER3 **Bits18**
1 = Terminal 3 NOT installed
0 = Terminal 3 installed
TER4 **Bits19**
1 = Terminal 4 NOT installed
0 = Terminal 4 installed

RESERVED **Bits20-27**

DTACK1 **Bits28**
1 = Terminal 1 Dtack timed out
DTACK2 **Bits29**
1 = Terminal 2 Dtack timed out
DTACK3 **Bits30**
1 = Terminal 3 Dtack timed out
DTACK4 **Bits31**
1 = Terminal 4 Dtack timed out

3.1.4 NHi-15650 TERMINAL MEMORY

The NHi-15650 memory is organized on 16 bit word boundaries. Registers are 16 bits wide and memory is stored as 16 bit words, therefore each address increment is one 16 bit word or two bytes..

When addressing the terminal via the PCI bus, double word addressing is used, therefore each address increment in a terminal is four bytes on the PCI bus. The PCI memory offset is therefore four times the desired internal memory address of the terminal plus the ident of the terminal.

PCI data is 32 bits wide, however only the lower 16 bits are used to transfer data to the terminal, the upper 16 bits should be set to '1'.

The PCI address to a Terminal is given by:
(PCI Base Address) + (Ident) + 4X(Internal Terminal Address).

The PCI address to the Card Register is given by:
(PCI Base Address) + (0XC0000).

The following table gives examples which illustrate the relationship between the PCI memory ident, offset. and the internal address of the NHi-156XX terminal.

Only type 0 addressing is recognized by the NHi-156XX PCI terminals. Address bits 0 and 1 of the PCI address/data bus must be set to "0" during the addressing phase of a command.

Pci Memory Offset	Ident	Terminal Int Addr	Function
00000000	0	0000	Control Reg
00000004	0	0001	Pntr Tbl Addr Reg
00100008	100000	0002	Basic Status Reg
0010002C	100000	000B	Last Cmd Reg
00100074	100000	001D	Log Pntr Tbl Reg
00100400	100000	0100	Terminal Ram
002048D0	200000	1234	Terminal Ram
0022EB44	200000	BAD1	Terminal Ram
00035FA4	300000	D7E9	Terminal Ram
0033FFFC	300000	FFFF	Terminal Ram

PCI address = (PCI Base Address) + (PCI Memory Offset).

3.1.5 PCI COMMANDS

Card uses a subset of the available PCI commands, all other PCI commands are not implemented. If the card receives a PCI command that is not implemented, it ignores the command and takes no action

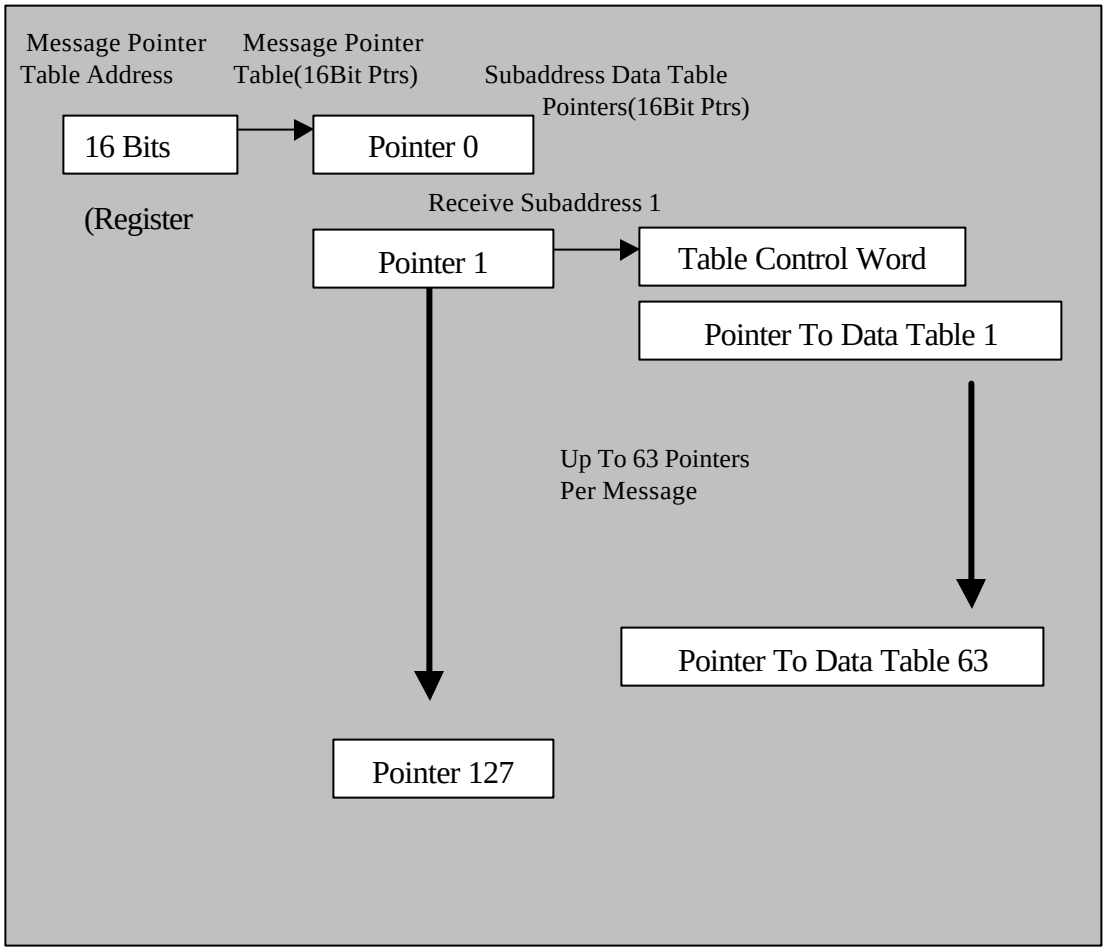
3.1.6 PCI COMMAND TABLE

CBE_3-0	COMMAND TYPE
0110	MEMORY READ
0111	MEMORY WRITE
1010	CONFIGURATION READ
1011	CONFIGURATION WRITE

The four PCI commands shown in this PCI Command Table are the only PCI commands implemented in the NHI-1505 CCPMC cards.

3.1.7 NHi-15505CCPMC MEMORY STRUCTURE

REMOTE TERMINAL MEMORY ORGANIZATION
The T/R bit subaddress and word count fields in the Command word are used to index into a message Pointer table as defined below:

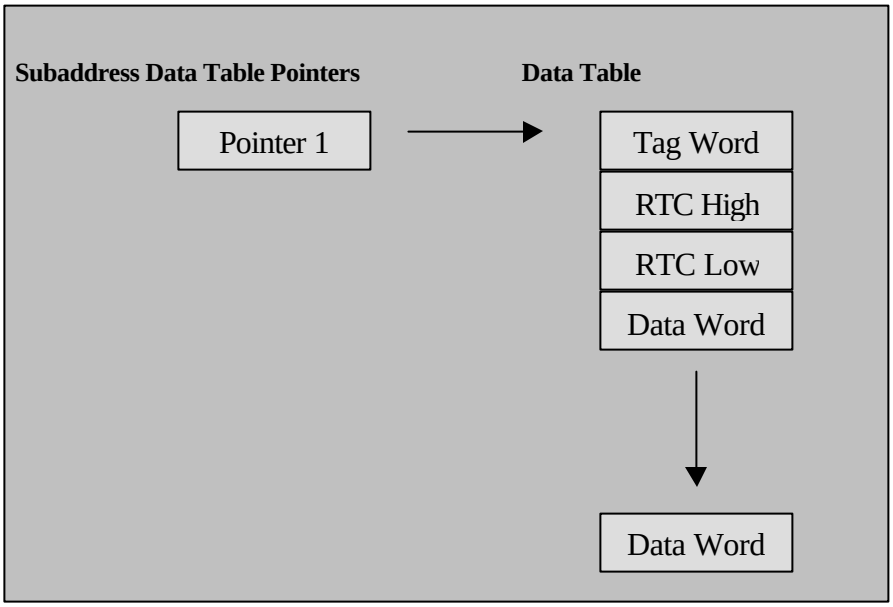


MESSAGE POINTER TABLE INDEX

Index	T/R	Subaddress	Mode Code	Command
0		**Not Used**		
1 - 30	**0**	**1 - 30**		**Receive/Bcst**
31	**0**	**31 (Note 2)**		**Receive/Bcst**
32		**Not Used**		
33 - 62	**1**	**1 - 30**		**Transmit**
63	**1**	**31 (Note 2)**		**Transmit**
64 - 95	**X**	**0,31 (Note 2)**	**0 - 31**	**Mode Code**
96		**Not Used**		
97 - 126	**0**	**1 - 30**		**Broadcast**
127	**0**	**31 (Note 2)**		**Broadcast**

Note : Broadcast messages may be separate or combined with Receive.

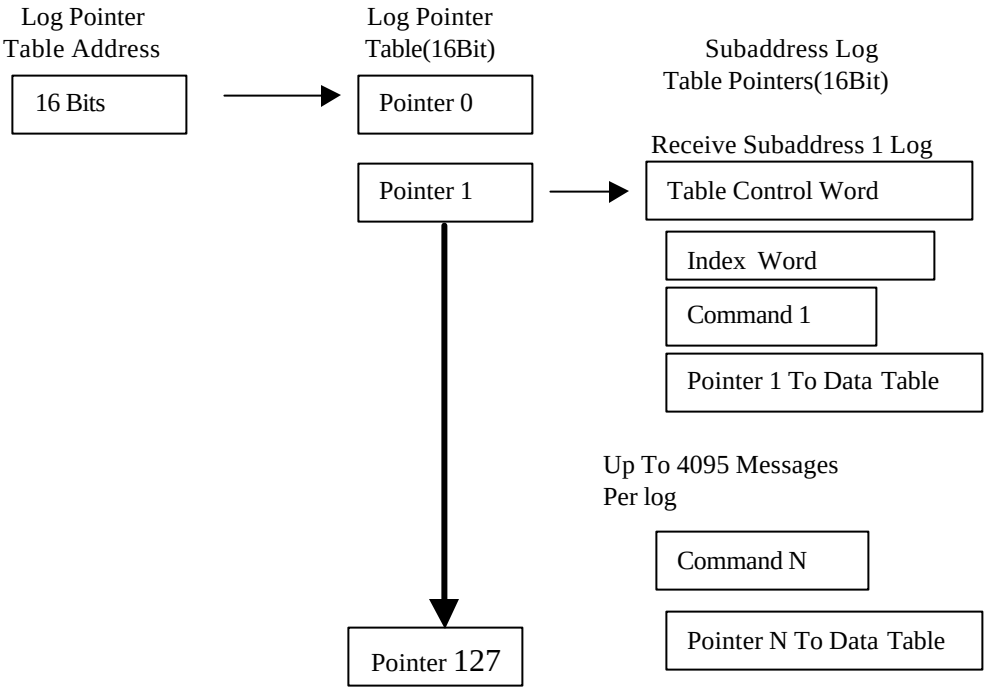
REMOTE TERMINAL DATA TABLE ORGANIZATION



REMOTE TERMINAL DATA TABLE TAG WORD

15	14	13	12	11	10	9	8
UPDATE	SSFENA	BCST	INTREQ	LOCATIO	PULSE2	PULSE1	PULSE0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK	INVALID	OVRWRT	WCNT4	WCNT3	WCNT2	WCNT1	WCNT0

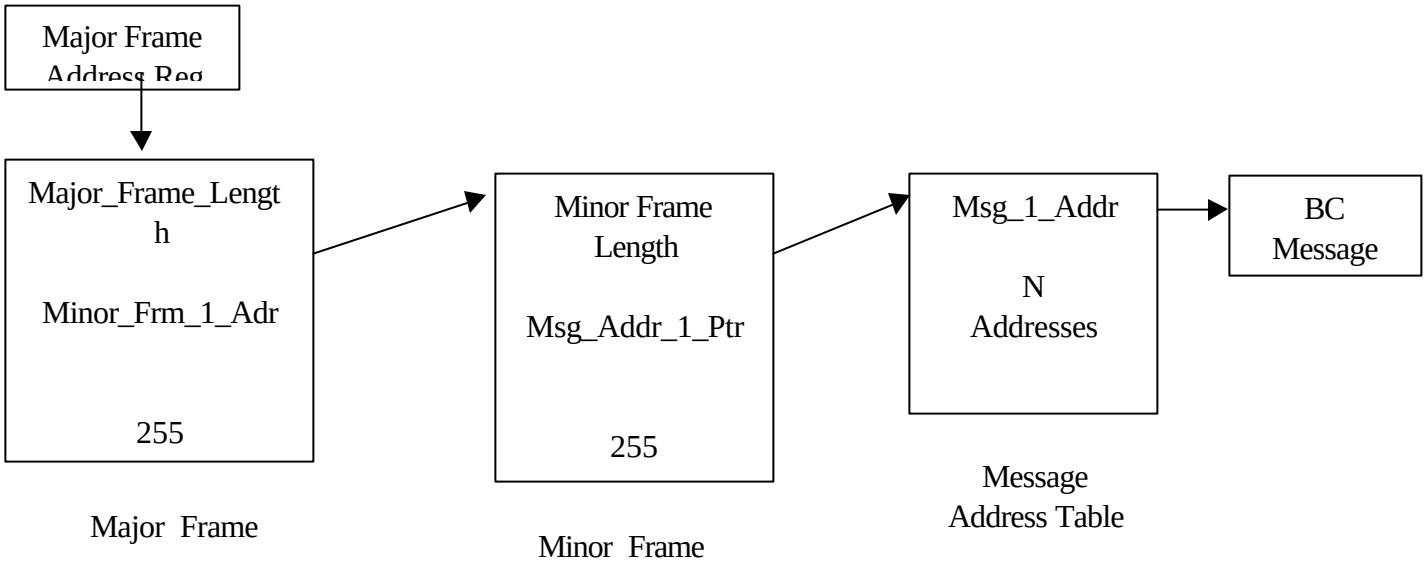
REMOTE TERMINAL MESSAGE LOG FORMAT



BUS CONTROLLER MEMORY ORGANIZATION

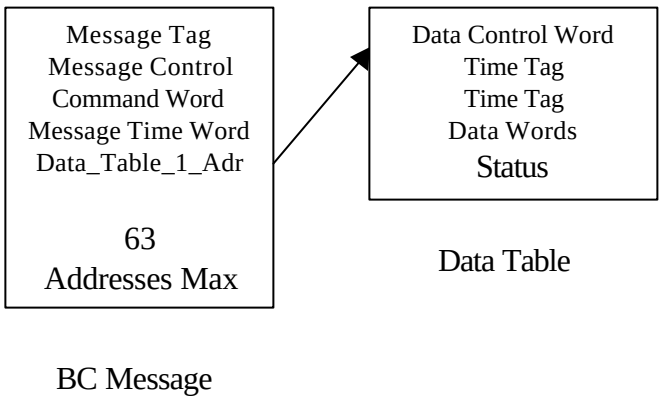
The message concept employs major and minor frames, message address tables, BC messages and data tables. This approach provides the BC with flexibility, autonomy and data buffering.

BCU FRAME STRUCTURE

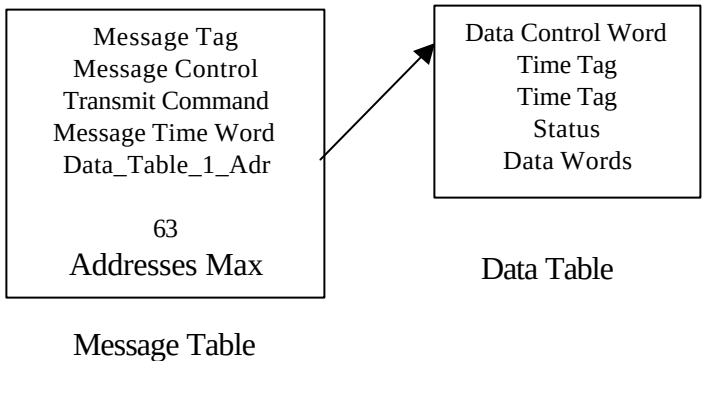


Message Structures

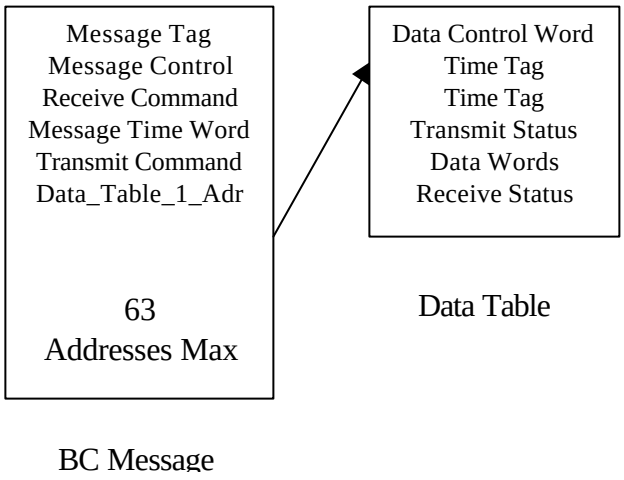
Receive Command



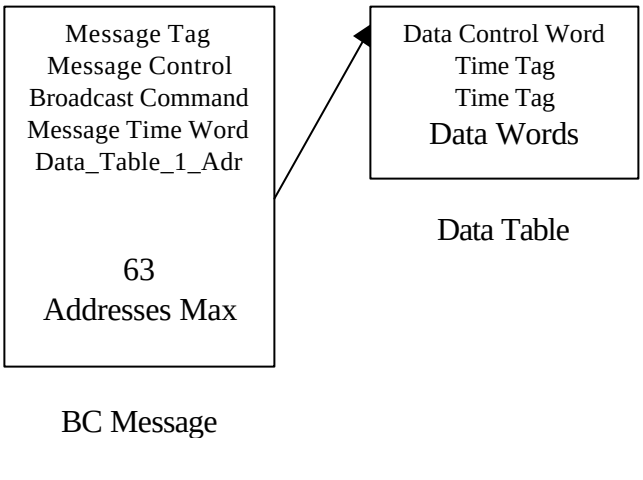
Transmit Command



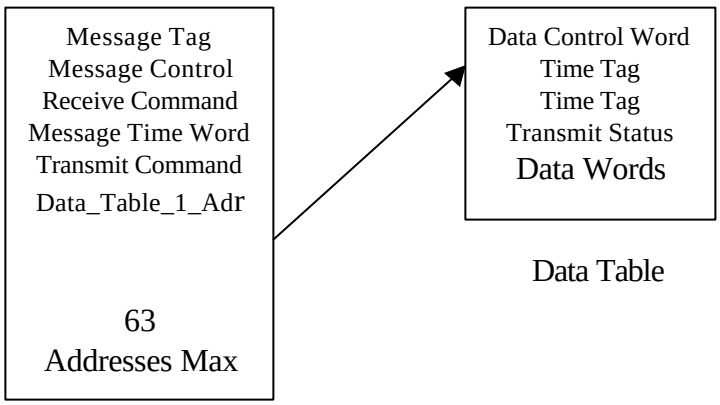
RT-RT Command



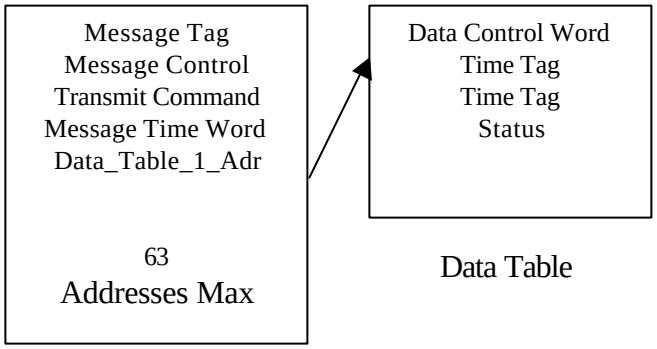
Broadcast Receive Command



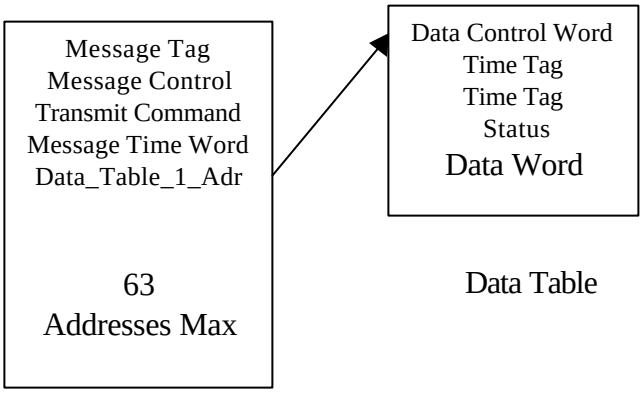
Broadcast RT-RT Command



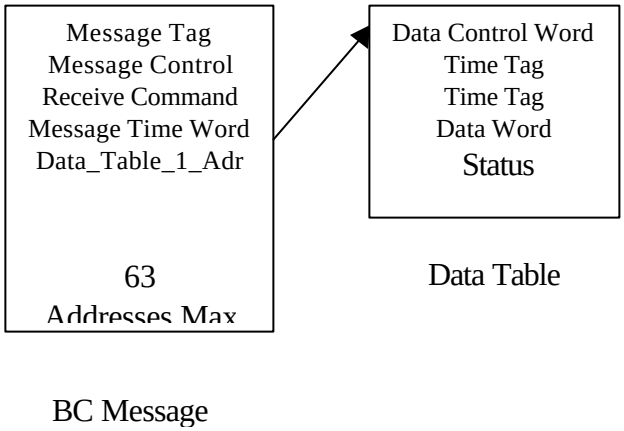
Transmit Mode Code - No Data



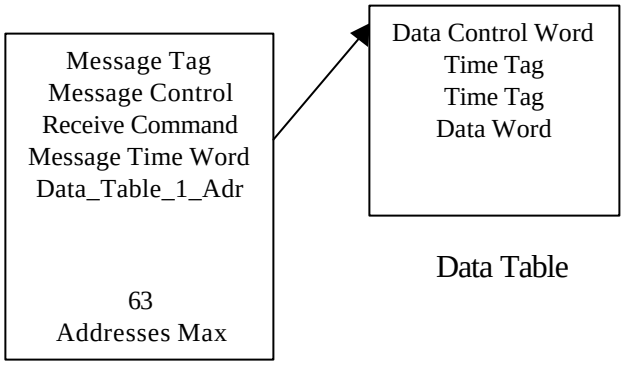
Transmit Mode Code + Data



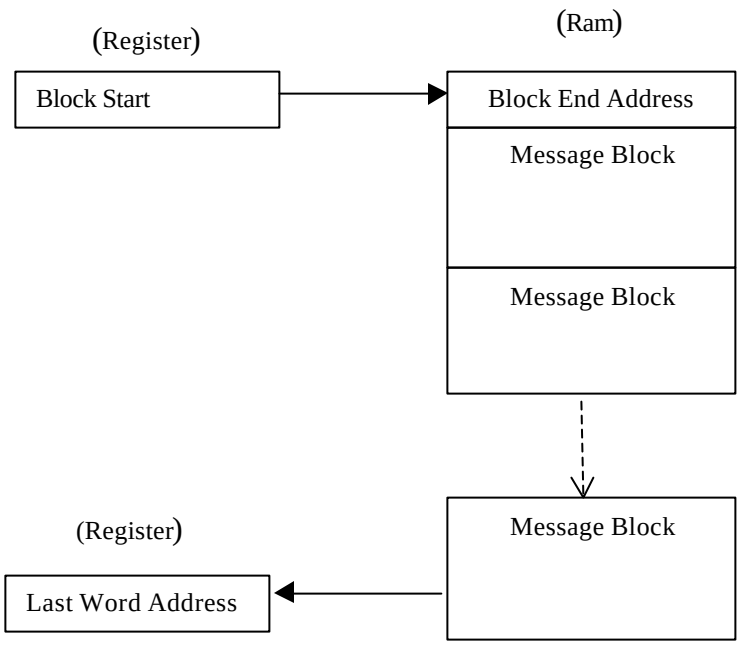
Receive Mode Code



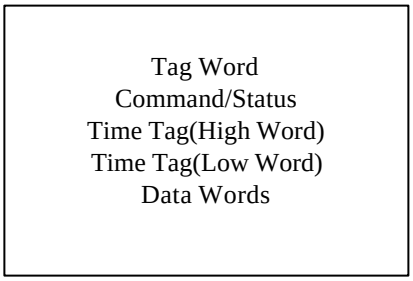
Broadcast Mode Code



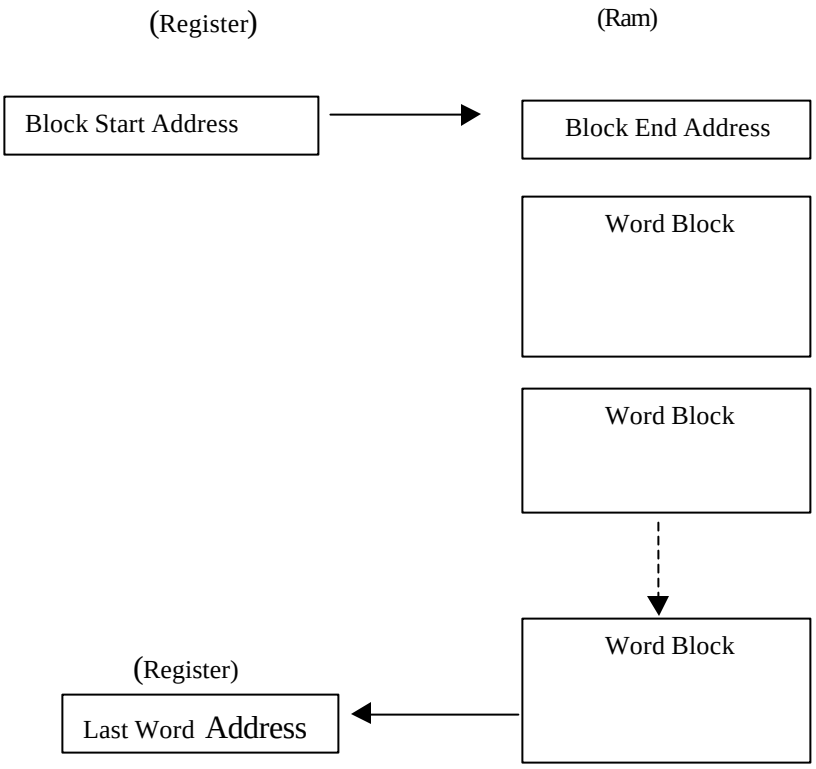
Message Monitor Structure



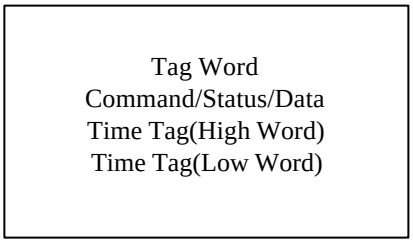
MESSAGE MONITOR MESSAGE BLOCK STRUCTURE



Word Monitor Structure



WORD MONITOR WORD BLOCK ORGANIZATION



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